Investigation of the Performance and Energy Consumption of Superconducting Adiabatic Computing Circuits

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Superconducting circuits using adiabatic quantum-flux-parametron (AQFP) logic have been shown to have ultra-low power consumption. The energy dissipation of adiabatic processes are orders of magnitude lower than non-adiabatic processes, which can lead to a high number of logic gates with little power consumption. We have studied the bit-energy dissipation of various superconducting computing circuits that use AQFP logic gates, including NOT gates and Full Adders. In digital binary computation, a NOT gate will give an output "1" when it has an input "0," and it will give an output "0" when it has an input "1." A Full Adder performs an addition operation on three one-bit binary numbers. It produces a sum of the three inputs and a carry value. AQFP logic gates use Josephson Junctions (JJs). These devices consist of a thin layer of non-superconducting material between two layers of superconducting material. When a critical level of current is reached, electron pairs can tunnel across the non-superconducting layer. This is known as the Josephson effect. We have analyzed numerous AQFP logic circuits using the JJ simulator, JSIM.

A NOT gate and Full Adder were separately tested in JSIM (Figures 1 and 2). First, these circuits were verified by testing all possible input combinations and examining the results. Once we confirmed that these circuits were operating correctly, we ran multiple bit-energy dissipation analyses tests. We simulated one bit of input, which correlated to one pulse for each excitation line in the circuit. The energy dissipated in the excitation lines was then calculated. For each consecutive test, the rise/fall time of the trapezoidal excitation current was increased by 10 ps. This process was repeated from 100 ps to 10,000 ps.

In AQFP logic, a NOT gate has two AQFP gates, where the output of the first is negatively coupled with the input of the second. The simulated energy dissipation for the excitation lines in this circuit leveled out with an increasing rise/fall time, well above $k_B T \ln 2$. This refers to the Landauer limit, or the thermal limit for one bit of information. These simulations assume an operating temperature of 4.2 °K, where the Landauer limit would be about 0.04 zJ. In AQFP logic, a Full Adder uses a MAJ gate, where the output corresponds to the majority values of the three inputs. Notably, this circuit had two excitation lines wherein the simulated energy dissipation decreased linearly with increasing rise/fall time, suggesting that they could fall below the Landauer limit with a greater rise/fall time.

In conclusion, we have successfully simulated a functional NOT gate and Full Adder using AQFP gates, which are two essential components of digital logic. The energy dissipation results of the Full Adder indicate that longer rise/fall times can lead to power consumption below the Landauer limit. This shows how AQFP logic could lead to a much greater energy efficiency than both the CMOS technology, which is currently used, and various other superconducting technologies, such as RSFQ and ASL.

Statement of Research Advisor

As we move towards new forms of computing, technologies based on superconductive devices are becoming more intriguing. The inherent, near-zero, power dissipation in superconductors presents opportunities for extremely low energy computing. Adiabatic digital logic circuits, such as the AQFP circuits studied here and other related technologies, are very promising for computing with ultra-high energy efficiency while also maintaining high operation speeds. The work presented here provides the foundation on which our future simulation and experimental efforts will be based.

– Michael Hamilton, Electrical and Computer Engineering

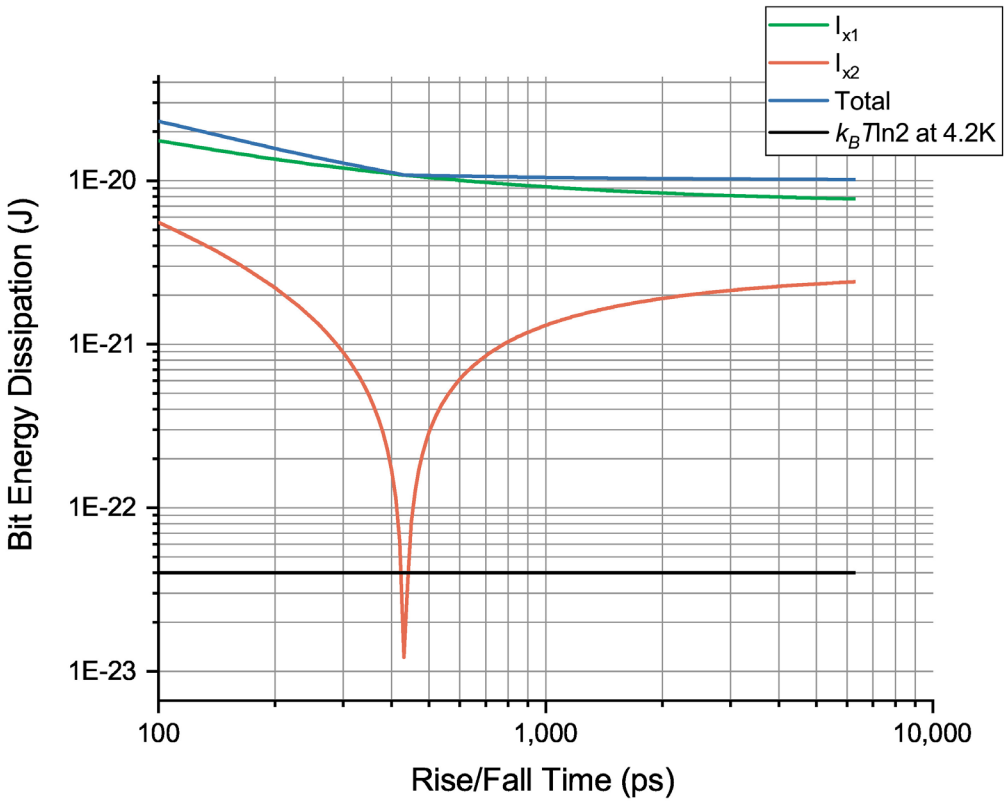

Figure 1: Simulation results from bit energy dissipation analysis of a NOT gate. I_{x1} and I_{x2} represent each excitation line in the circuit, *Total* represents the combined energy dissipated in all excitation lines, and $k_BT\ln 2$ at 4.2 °K represents the Landauer limit.

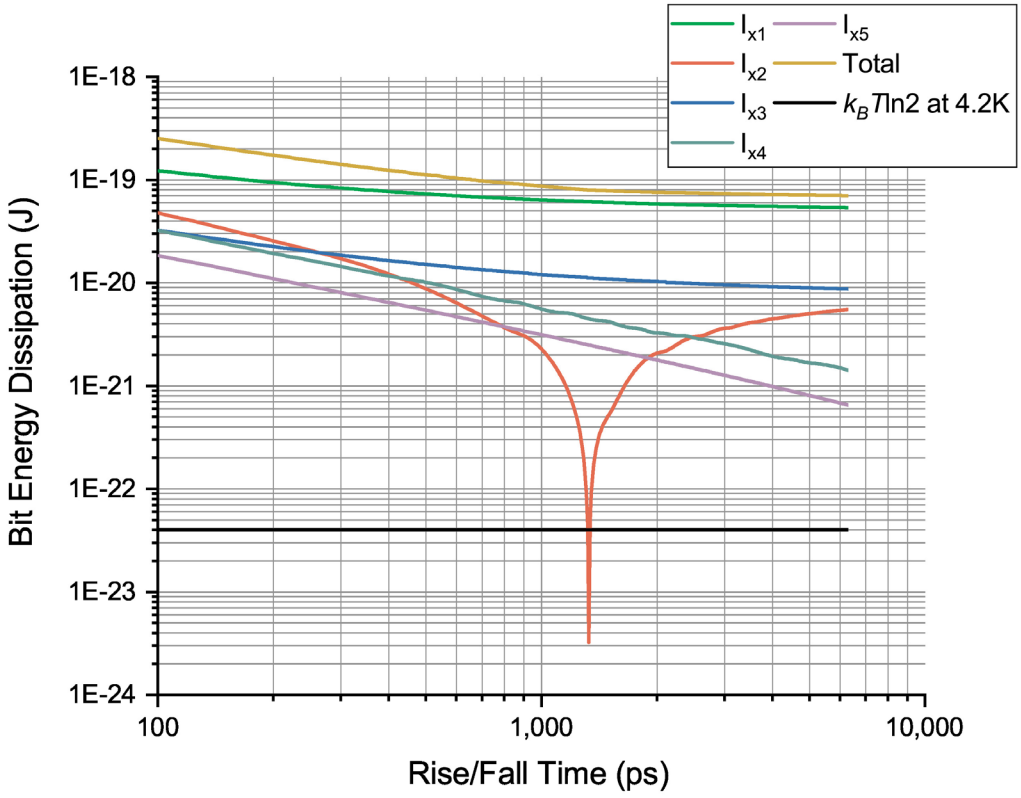

Figure 2: Simulation results from bit energy dissipation analysis of a Full Adder. I*x1*-I*x5* represent each excitation line in the circuit, *Total* represents the combined energy dissipated in all excitation lines, and $k_BT\ln 2$ at 4.2 °K represents the Landauer limit.